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AMENDMENTS TO THE SPECIFICATION

Please replace Paragraph [0001] with the following amended paragraph:

[0001] This application is related to the following commonly-
owned, co-pending U.S. Patent Applications: U.S. Patent
Application No. 10/803,715 [[]], filed March 18, 2004,
[[]] entitled "SYSTEM AND METHOD TO OPTIMIZE LOGICAL
CONFIGURATION RELATIONSHIPS IN VLSI CIRCUIT ANALYSIS TOOLS" (Docket
No. 200311735-1); U.S. Patent Application No. 10/803,692 [[
]], filed <u>March 18, 2004,</u> [[]] entitled "SYSTEM AND
METHOD FOR FACILITATING EFFICIENT APPLICATION OF LOGICAL
CONFIGURATION INFORMATION IN VLSI CIRCUIT ANALYSIS TOOLS" (Docket
No. 200311736-1); U.S. Patent Application No. <u>10/803,610</u>
[[]], filed <u>March 18, 2004,</u> [[]] entitled
"SYSTEM AND METHOD TO PRIORITIZE AND SELECTIVELY APPLY
CONFIGURATION INFORMATION FOR VLSI CIRCUIT ANALYSIS TOOLS" (Docket
No. 200311762-1); U.S. Patent Application No. <u>10/803,561</u>
[[]], filed <u>March 18, 2004,</u> [[]] entitled
"SYSTEM AND METHOD FOR CONTROLLING ANALYSIS OF MULTIPLE

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INSTANTIATIONS OF CIRCUITS IN HIERARCHICAL VLSI CIRCUIT DESIGNS"
(Docket No. 200311778-1); and U.S. Patent Application No.
10/803,714 [[]], filed March 18, 2004, [[]]
entitled "SYSTEM AND METHOD TO LIMIT RUNTIME OF VLSI CIRCUIT
ANALYSIS TOOLS FOR COMPLEX ELECTRONIC CIRCUITS" (Docket No.
200311780-1); all of which are hereby incorporated by reference in
their entirety.

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Please replace Paragraph [0034] with the following amended paragraph:

[0034] In addition to combining all of the configuration information together in a per-net fashion, the Configuration Generation module 408 also propagates some logic configuration through a process referred to as "transitive closure", as described in related U.S. Patent Application No. 10/803,715 [[_____]] (Docket No. 200311735-1), which has been incorporated by reference in its entirety.